(12) UK Patent Application (19) GB (11) 2 167 899 A

(43) Application published 4 Jun 1986

(21) Application No 8527737

(22) Date of filing 11 Nov 1985

(30) Priority data
(31) 59/241239 (32) 15 Nov 1984 (33) JP

(71) Applicant
Sony Corporation (Japan),
6–7–35 Kitashinagawa, Shinagawa-ku, Tokyo 141, Japan

(72) Inventors
Hisao Hayashi
Takashi Noguchi

(74) Agent and/or Address for Service
D Young & Co,
10 Staple Inn, London WC1V 7RD

(51) INT CL⁴
H01L 21/18 21/265 21/324 29/78

(52) Domestic classification (Edition H):
H1K 1CA 4C11 4C14 4H1A 4H3X 9C2 9C3 9D1 9N2 9N3 9R1 CAA

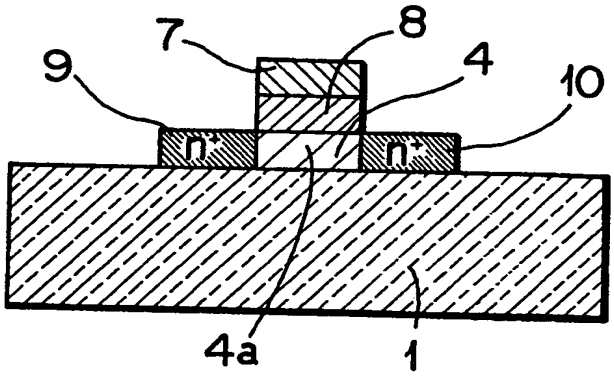
(56) Documents cited
None

(58) Field of search
H1K
Selected US specifications from IPC sub-class H01L

(54) Method of manufacturing thin film transistors

(57) A method of manufacturing a thin film transistor comprises forming a thin polycrystalline semiconductor film 4 on a substrate 1, implanting ions in the thin polycrystalline semiconductor film to form a thin amorphous semiconductor film, forming a gate insulating film 8 and a gate electrode 7 on the thin amorphous semiconductor film, doping impurities for forming source and drain regions 9,10 in the thin amorphous semiconductor film using the gate electrode 7 and the gate insulating film 8 as masks, and performing annealing for solid-phase growing the thin amorphous semiconductor film and at the same time for electrically activating the impurities to form the source and drain regions 9,10.

FIG. 2C



GB 2 167 899 A

2167899

FIG. 1A

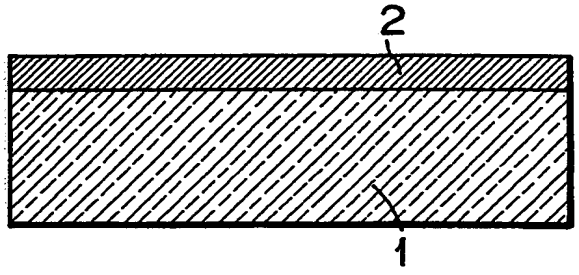


FIG. 1B

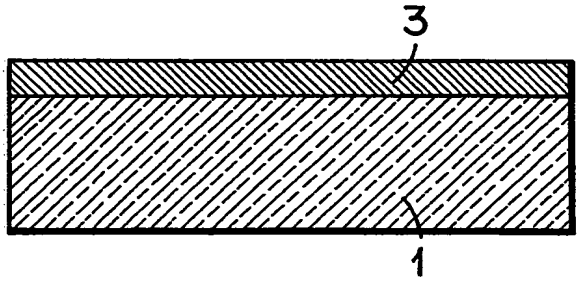


FIG. 1C

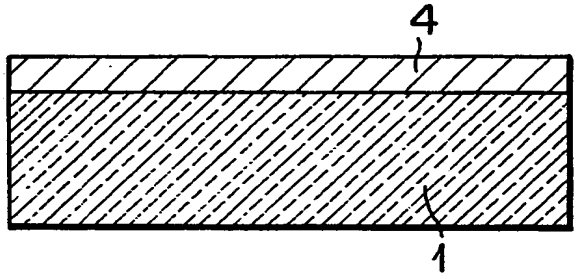
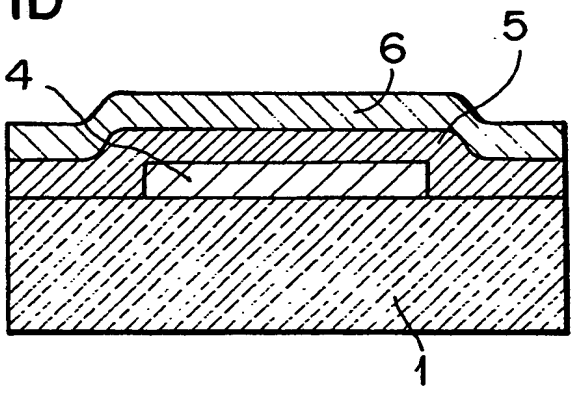


FIG. 1D



2167899

FIG. 1E

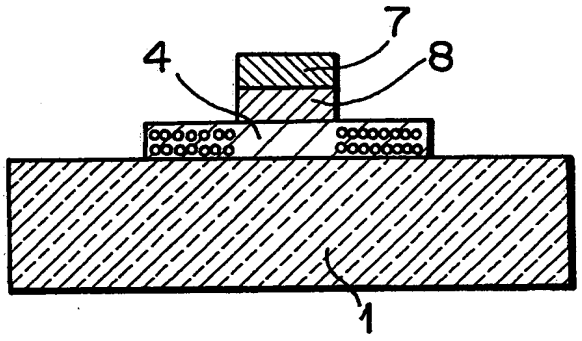


FIG. 1F

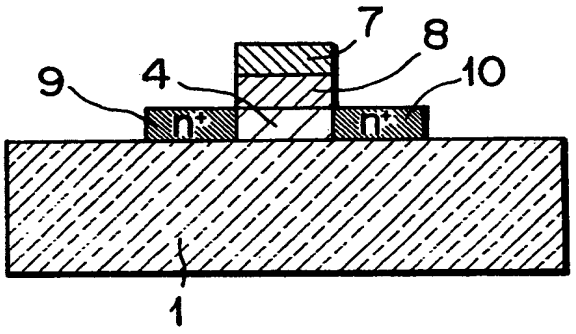


FIG. 1G

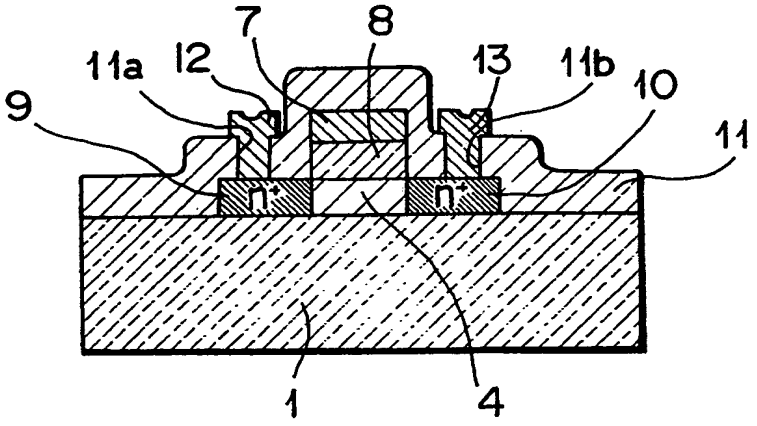


FIG. 2A

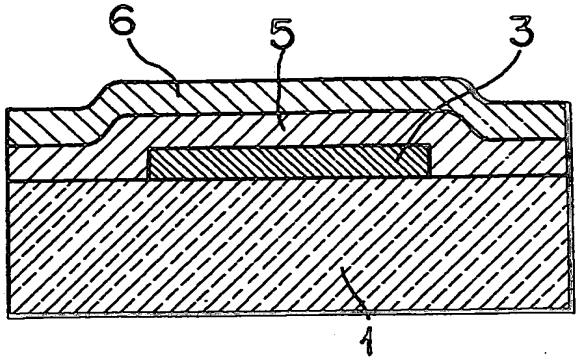


FIG. 2B

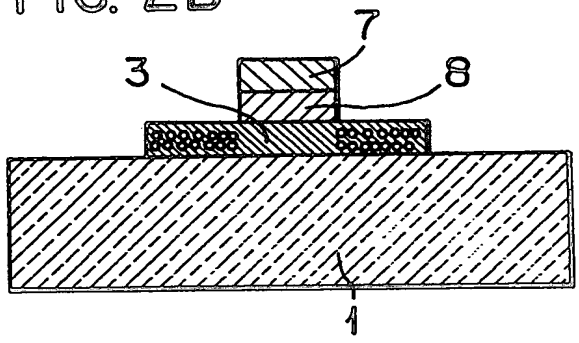
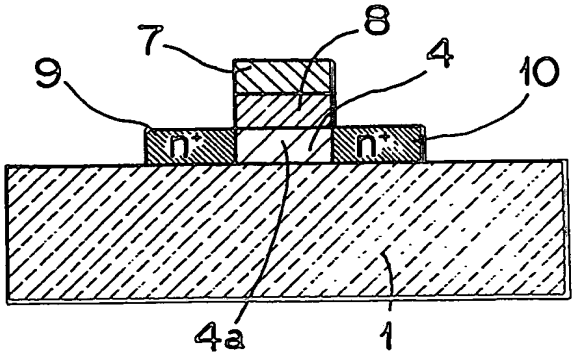


FIG. 2C



SPECIFICATION

Methods of manufacturing thin film transistors

This invention relates to methods of manufacturing thin film transistors (TFTs), and TFTs manufactured by such methods.

A polysilicon TFT has been manufactured in a low-temperature process as follows. As shown in Fig. 1A of the accompanying drawings, a polysilicon film 2 is deposited by a low-pressure chemical vapour deposition (LPCVD) method on a glass substrate 1 at a temperature of 600°C or less. The glass substrate has a melting point of, for example, about 680°C. Ions of an electrically inactive element, such as silicon Si⁺ ions, are implanted in the polysilicon film 2 to form an amorphous silicon film 3, as shown in Fig. 1B of the accompanying drawings. The resulting structure is annealed at a temperature of 500°C to 600°C to solid-phase grow the amorphous Si film 3, so that the amorphous Si film 3 is crystallized. As a result, a polysilicon film 4 having a larger crystal grain size (not shown) than that of the polysilicon film 2 is formed, as shown in Fig. 1C of the accompanying drawings. As shown in Fig. 1D of the accompanying drawings, a predetermined portion of the polysilicon film 4 is etched to obtain a predetermined pattern. A silicon dioxide (SiO_2) film 5 is then deposited by chemical vapour deposition (CVD) at a temperature of about 400°C to cover the entire surface of the resulting structure. Subsequently, a film such as molybdenum (Mo) film 6 is sputtered on the SiO_2 film 5. Predetermined portions of the Mo and SiO_2 films 6 and 5 are sequentially etched to form a Mo gate electrode 7 with a predetermined pattern and a gate insulating film 8 comprising a SiO_2 pattern which is the same as that of the Mo gate electrode 7. Subsequently, n-type impurities such as phosphorus (P) are ion-implanted in the polysilicon film 4 at a high concentration by using as masks the gate electrode 7 and the gate insulating film 8 (the P ions in the polysilicon film 4 are represented by hollow dots in Fig. 1E of the accompanying drawings). The resulting structure is annealed at a temperature of about 600°C to electrically activate the impurities, thereby forming n⁺ type source and drain regions 9 and 10, as shown in Fig. 1F of the accompanying drawings. As shown in Fig. 1G of the accompanying drawings, a SiO_2 film 11 is deposited by the CVD method as a passivation film at a temperture of about 400°C to cover the entire surface. Subsequently, predetermined portions of the SiO_2 film 11 are etched to form contact holes 11a and 11b. Aluminium is deposited to cover the entire surface and is etched to form electrodes 12 and 13 in the contact holes 11a and 11b, thereby forming an n-channel polysilicon TFT.

This method of manufacturing a polysilicon TFT by a low-temperature process has the following drawback. Annealing for solid-phase growing the amosphous Si film 3 must be separated from annealing for electrically activating the impurities to form the source and drain regions 9 and 10, and thus the fabrication process is complicated. Furthermore, although part of the ion-implanted impurities in the polysilicon film 4 is present at grain boundaries in the polysilicon film 4, it is difficult to electrically activate the impurities present in the grain boundaries by annealing. Therefore, the total activation efficiency of the impurities is low. The doped impurity ions are inevitably subjected to channelling to some extent upon ion-implantation of the impurities in the polysilison film 4. Therefore, during subsequent annealing, the impurities in the source and drain regions 9 and 10 cannot be uniformly activated.

A prior art TFT reference is exemplified in the 45th Lecture Articles of the Japan Society of Applied Physics (1984), Nos. 14p-A-4 to 14p-A-6, pp 407–408. This reference describes a polysilicon TFT having the transistor characteristics improved by an ultra-thin polysilicon film, improvements in a solid-phase crystal grain growth effect and conduction characteristics of the ultra-thin polysilicon film obtained by thermal oxidation, and an improvement in transistor characteristics obtained by annealing a structure in a hydrogen atmosphere at a temperature of 400° after a silicon nitride (Si_3N_4) film has been formed by a plasma CVD method on the ultra-thin polysilicon TFT to obtain the structure.

According to the present invention there is provided a method of manufacturing a thin film transistor, comprising the steps of: forming a thin polycrystalline semiconductor film on a substrate;
implanting ions in said thin polycrystalline semiconductor film to form a thin amorphous semiconductor film;
forming a gate insulting film and a gate electrode on said thin amorphous semiconductor film;
doping impurities for forming source and drain regions in said thin amorphous semiconductor film by using said gate electrode and said gate insulating film as masks; and
performing annealing for solid-phase growing said thin amorphous semiconductor film and at the same time for electrically activating the impurities to form said source and drain regions.

With such a method, annealing for solid-phase growing the thin amorphous semiconductor film need not be separated from annealing for electrically activating the impurities for forming the source and drain regions. The fabrication process can thus be simplified. In addition, the impurities in the source and drain regions can be uniformly activated as com-

pared with conventional transistors.

The invention will now be described by way of example with reference to the accompanying drawings, throughout which like parts are referred to by like references, in which:

Figures 1A to 1G are sectional views for explaining the steps in manufacturing a polysilicon TFT by a prior low-temperature method; and

Figures 2A to 2C are sectional views for explaining the steps in manufacturing an n-channel polysilicon TFT by a method according to the present invention.

A method of manufacturing a polysilicon TFT and according to the present invention will now be described with reference to Figs. 2A to 2C of the accompanying drawings. As the same reference numerals in Figs. 2A to 2C denote the same parts as in Figs. 1A to 1G, a detailed description thereof will be omitted.

A polysilicon film 2 having a thickness of, for example, 800 Angstroms is deposited by a LPCVD method on a glass substrate 1 at a temperature of about 580°C to 600°C in the same manner as in Fig. 1A. $Si^{\cdot}$ ions are implanted in the polysilicon film 2 at an acceleration energy of 40 keV and a dose of $1\times10^{15}cm^{-2}$ $5\times10^{15}cm^{-2}$ to form an amorphous Si film 3 in the same manner as in Fig. 1B.

As shown in Fig. 2A, a predetermined portion of the amorphous Si film 3 is etched to obtain a predetermined pattern. A SiO_2 film 5 having a thickness of, for example, 1000 Angstroms is deposited by a LPCVD method on the entire exposed surface in the same manner as in Fig. 1D. A Mo film 6 having a thickness of, for example, 3000 Angstroms is sputtered on the surface of the SiO_2 film 5.

As shown in Fig. 2B, predetermined portions of the Mo and SiO_2 films 6 and 5 are sequentially etched to form a gate electrode 7 and a gate insulating film 8 in the same manner as in Fig. 1E. Thereafter, $P^{\cdot}$ ions are implanted in the amorphous silicon film 3 by using as masks the gate electrode 7 and the gate insulating film 8 (the P ions in the amorphous Si film 3 are represented by hollow dots in Fig. 2B).

Annealing is performed at a temperature of about 600°C to solid-phase grow the amorphous Si film 3 to form a polysilicon film 4, as shown in Fig. 2C. At the same time, the doped P ions are electrically activated to form $n^{\cdot}$ type source and drain regions 9 and 10. Thereafter, a SiO_2 film 11 as a passivation film and electrodes 12 and 13 are formed to complete an n-channel polysilicon TFT in the same manner as in Fig. 1G.

As described above, solid-phase growth of the amorphous Si film 3 and activation of the impurities for forming the source and drain regions 9 and 10 can be performed by a single annealing. Therefore, as compared with the prior method shown in Figs. 1A to 1G, one annealing step can be omitted, thereby simplifying the fabrication process. In the annealing process described above, solid-phase growth of the amorphous Si film 3 is simultaneously performed with activation of the implanted impurities. Therefore, the impurities in the source and drain regions 9 and 10 can be uniformly activated.

In the annealing process described above, crystal nuclei tend to be performed at the P ion implanted region in the amorphous Si film 3 upon solid-phase growth of the amorphous Si film 3. These nuclei grow into small crystals and then into large crystals grains, thereby increasing the size of the crystal grains in the source and drain regions 9 and 10 as compared with the prior transistor. Therefore, since the area of the grain boundaries is decreased as compared with that in the prior transistor, the impurities can be activated effectively to an extent corresponding to a decrease in the area of the grain boundaries. By using the small crystals as crystal seeds, crystal growth progresses along a direction parallel to the surface of the amorphous Si film 3. The size of crystal grains in the polysilicon film 4 obtained by the solid-phase growth described above in a channel region 4a (Fig. 2C) is larger than that in the prior transistor. A channel is formed in the channel region upon operation of the TFT. Therefore, carrier mobility of the TFT is improved as compared with that of the prior TFT.

With this method, since the impurities are ion-implanted to form the source and drain regions 9 and 10 after the polysilicon film 2 has been implanted with $Si^{\cdot}$ ions to form the amorphous Si film 3, channelling of the implanted impurities does not occur substantially. The implanted impurity profile of the TFT is more uniform that that of the prior TFT. Therefore, the impurities in the source and drain regions 9 and 10 can be more uniformly activated that that in the conventional TFT.

Various changes and modifications can be made. For example, ions of an electrically inactive element such as fluorine ($F^{\cdot}$) may be used in place of $Si^{\cdot}$ used as the ion implantation source for converting the polysilicon film 2 to the amorphous Si film 3. The ion implantation source for forming the source and drain regions 9 and 10 is not limited to $P^{\cdot}$ either, but can be extended to ions of other elements as needed. Furthermore, the material of the gate electrode 7 may comprise another refractory metal such as tungsten (W), or a refractory metal silicide. The polysilicon film 2 may be replaced with another thin polycrystalline semiconductor film. The polysilicon film 2 may be formed by another method such as a glow discharge decomposition method (plasma CVD method) in place of the LPCVD method. With the glow discharge decomposition method, a polysilicon film 2 can be formed at a tempera-

ture of about 200°C or less.

CLAIMS

1. A method of manufacturing a thin film transistor, comprising the steps of:
forming a thin polycrystalline semiconductor film on a substrate;
implanting ions in said thin polycrystalline semiconductor film to form a thin amorphous semiconductor film;
forming a gate insulating film and a gate electrode on said thin amorphous semiconductor film;
doping impurities for forming source and drain regions in said thin amorphous semiconductor film by using said gate electrode and said gate insulating film as masks; and
performing appealing for solid-phase growing said thin amorphous semiconductor film and at the same time for electrically activating the impurities to form said source and drain regions.

2. A method according to claim 1 wherein said thin polycrystalline semiconductor film comprises a polysilicon film.

3. A method according to claim 2 wherein said ions comprise Si^{+} ions at a dose of 1×10^{15} cm $^{-2}$ to 5×10^{15} cm $^{-2}$.

4. A method according to claim 2 or claim 3 wherein said polysilicon film is formed by low-pressure chemical vapour deposition at a substrate temperature of 580°C to 600°C.

5. A method according to any one of the preceding claims wherein said substrate is glass.

6. A method of manufacturing a thin film transistor, the method being substantially as hereinbefore described with reference to Figs. 2A to 2C.

7. A thin film transistor made by a method according to any one of the preceding claims.

Printed in the United Kingdom for
Her Majesty's Stationery Office, Dd 8818935, 1986, 4235.
Published at The Patent Office, 25 Southampton Buildings,
London, WC2A 1AY, from which copies may be obtained.